

VT-RT6M

Bluetooth® Low Energy Mesh Module

Version 0.6BETA Preliminary Release

INTRODUCTION

VT-RT6M is an ultra-low-power SoC module for Bluetooth[®] 5.0 low energy applications that combines the excellent performance of a leading RF transceiver with a low-power ARM[®] Cortex-M4F and rich powerful supporting features and peripherals. The VT-RT6M supports Bluetooth® mesh networking specification suited for largescale device networks to support building automation, sensor networks, asset tracking and other solutions where multiple devices need to communicate reliably and securely.

FEATURES

- Bluetooth® Core Spec v5.0 compliant
- Supports Bluetooth Mesh Networking Specification
- Supports AES128/192/256 encryption/decryption
- Supports OTA (Over-the-Air) for firmware upgrade

•	Battery Supply Voltage	1.8V to 3.6V
•	Operational Temperature	-30°C to +85°C

Current Consumptions

Power Down Mode	450nA (Typ.)
Deep LPS (with 160K SRAM retention) Mode	2.5uA (Typ.)
TX Mode (+0dBm)	8.4mA (Typ.)
TX Mode (+4dBm)	10.4mA (Typ.)
TX Mode (+8dBm)	12.7mA (Typ.)
RX Mode	6.8mA (Typ.)

- Radio Bluetooth® Qualification (End Product, QDID: TBD)
- Meets Radio Certification FCC, RED, KCC and MIC Japan
- 11.05mm(W) x 17.0mm(L) x 2.1mm(H) Dimension
- Pb Free, RoHS Compliant



REVERSION HISTORY

Version Code	Date	Descriptions
0.52 BETA	7-MAY-19	Preliminary release
0.53 BETA	6-JUN-19	Change module part no.;
U.33 BETA	0-JUN-19	Update operational temperature range;
	4-SEP-19	Add module block diagram;
		Add AT Command mode pin definitions;
0.60 BETA		Add module interface descriptions;
		Add module electrical characteristics;
		Add PCB layout guide;
1.0	21-Dec-20	Add RF certifications

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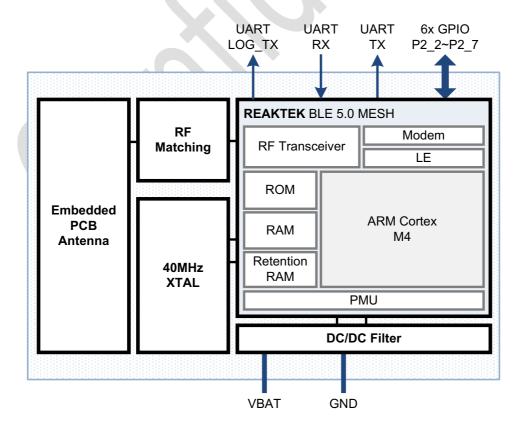
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MODULE SPECIFICATIONS

Specificat	ion Name	Descriptions
Module Dimension		11.05mm(W) x 17mm(L) x 2.1mm(H)
BLE Core Compliant		BLE V5.0
Operation Distance		Up to 80Meters (*LE 1M, apple to apple testing results)
Power Supply		1.8V – 3.6V
	Power Down Mode	450nA
	Deep LPS	2.5uA
Davis Caracina atian	TX mode (+0dBm)	8.4mA
Power Consumption	TX mode (+4dBm)	10.4mA
	TX mode (+8dBm)	12.7mA
	RX mode	6.8mA
Antenna Type		embedded PCB antenna
GPIO Numbers: PWM Numbers:		Up to 8x (including P3_0 and P3_1)
		Up to 6x (P2_2 to P2_7)
12bit ADC Numbers:		Up to 6x (P2_2 to P2_7)
Support interfaces		UART/4-wire SPI master/4-wire SPI slave

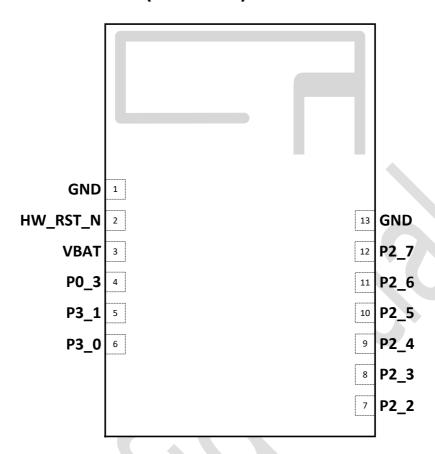
■ BLOCK DIAGRAM



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PIN ASSIGNMENTS (TOP VIEW)



PIN DEFINITIONS

SoC Mode Condition:

Note: INOUT (digital bidirectional), ANA(analog pin), DIG(digital pin).

#	Pin Name	I/O	Ana/Dig	Function					
1	GND	-	GND	GND					
2	HW_RST_N	IN	DIG	Hardware reset pin; low active;					
3	VBAT	-	PWR	Power Supply, 1.8V to 3.6V;					
4	P0_3	OUT	DIG	LOG_UART_TX (default)					
5	P3_1	INOUT	DIG	HCI_UART_RX (default) General purpose IO, 8mA driving capability; With wakeup function, internal strong/weak pull-up and pull-down;					
6	P3_0	INOUT	DIG	HCI_UART_TX (default) General purpose IO, 8mA driving capability; With wakeup function, internal strong/weak pull-up and pull-down;					



			·
	INOUT	ANA/DIG	AUXADC input 2 (default)
P2 2			General purpose IO, 8mA driving capability;
_		,	With wakeup function, internal strong/weak pull-up and pull-
			down;
			AUXADC input 3 (default)
ר בח	INOLIT	ANA/DIC	General purpose IO, 8mA driving capability;
P2_3	INOUT	ANAJDIG	With wakeup function, internal strong/weak pull-up and pull-
			down;
			AUXADC input 4 (default)
			General purpose IO, 8mA driving capability;
9 P2_4	INOUT	ANA/DIG	With wakeup function, internal strong/weak pull-up and pull-
			down;
			AUXADC input 5 (default)
D2 F	INOUT	ANA/DIG	General purpose IO, 8mA driving capability;
P2_5			With wakeup function, internal strong/weak pull-up and pull-
			down;
			AUXADC input 6 (default)
	INOUT	ANA/DIG	General purpose IO, 8mA driving capability;
P2_6			With wakeup function, internal strong/weak pull-up and pull-
			down;
			AUXADC input 7 (default)
D2 7	INOUT	ANIA /DIC	General purpose IO, 8mA driving capability;
P2_/		ANA/DIG	With wakeup function, internal strong/weak pull-up and pull-
			down;
GND	-	GND	GND
	P2_2 P2_3 P2_4 P2_5 P2_6 P2_7	P2_3 INOUT P2_4 INOUT P2_5 INOUT P2_6 INOUT P2_7 INOUT	P2_3 INOUT ANA/DIG P2_4 INOUT ANA/DIG P2_5 INOUT ANA/DIG P2_6 INOUT ANA/DIG

UART AT Command Mode Condition:

Note: ANA(analog pin), DIG(digital pin).

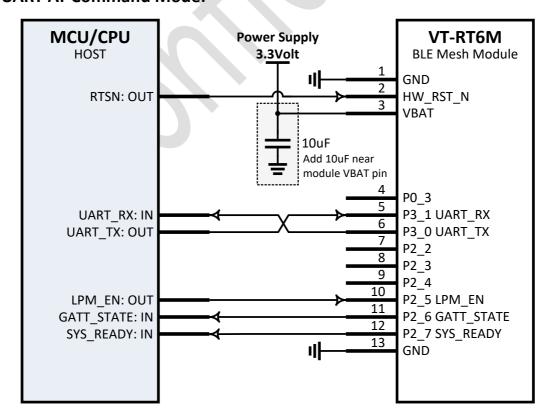
#	Pin Name	I/O	Ana/Dig	Function
1	GND	-	GND	GND
2	HW_RST_N	IN	DIG	Hardware reset pin; low active;
3	VBAT	-	PWR	Power Supply, 1.8V to 3.6V;
4	P0_3	OUT	DIG	LOG_UART_TX (default) for debugging purposed;
	_			Keep floating for general usage;
5	P3 1	IN	DIG	UART_RX;
				With weakly pull-high;
6	P3_0	OUT	DIG	UART_TX;



13	GND	-	GND	GND
				Output low when BLE stack not ready;
12	F Z_ /	001	סוט	Output high when BLE stack ready;
12	P2_7	OUT	DIG	indication pin for BLE stack ready;
		-		SYS_READY;
				Output low when disconnected;
11	P2_6	OUT	DIG	Output high when connected;
11	D2 C			Indication pin for GATT connection state;
				GATT_STATE;
				With weakly pull-low;
10	P2_5	IN	DIG	Enable low power mode, high active;
				LPM_EN;
9	P2_4	IN	ANA	With weakly pull-low;
				NC, keep floating for general usage;
8	P2_3	IN	ANA	With weakly pull-low;
				NC, keep floating for general usage;
7	P2_2	IN	ANA	With weakly pull-low;
	22.2			NC, keep floating for general usage;

■ APPLICATION EXAMPLE

UART AT Command Mode:



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INTERFACE DESCRIPTIONS

UART

VT-RT6M provides multiple UART baud-rate. The common baud-rate is shown in below table. The UART clock error between two devices should be less than +/- 2.5%.

VT-RT6M UART Features:

- Supports 7/8 data format.
- 1/2 bit stop bit.
- Configurable parity bit: odd/even.
- Programmable baud rate (maximum baud rate=4Mbps).
- Support hardware flow control.
- RX line idle state detect.
- DMA supported.

Baud-rate (bps)	Error (%)	Baud-rate (bps)	Error (%)
1200	-0.23	460800	0.17
9600	< 0.01	500000	< 0.01
14400	< 0.01	921600	0.18
19200	< 0.01	1000000	< 0.01
28800	< 0.01	1382400	0.17
38400	< 0.01	1444400	-0.31
57600	< 0.01	1500000	< 0.01
76800	0.01	1843200	-0.35
115200	< 0.01	2000000	0.02
128000	0.02	2764800	0.14
153600	-0.1	3000000	0.06
230400	0.03	400000	0.03

Table: UART Baud Rate



ELECTRICAL CHARACTERISTICS

Temperature Limit Ratings

Parameter	Description	Note	Min.	Тур.	Max.	Unit
T _{STORE}	Storage temperature		-55		125	°C
T _{AOP}	Operational Temperature		-30		85	°C

Power Supply DC Characteristics

Parameter	Description	Note	Min.	Тур.	Max.	Unit
V_{BAT}	Supply Voltage		1.8	3	3.6	V

ESD Characteristics

Parameter	Description	Note	Min.	Тур.	Max.	Unit
ESD _{HBM}	ESD, human body mode	All pins, test method: JESD22			3500	V
ESD _{MM}	ESD, machine mode	All pins, test method: JESD22			200	V
ESD _{CDM}	ESD, charged device mode	All pins, test method: JESD22			500	V

12bit-AUX ADC Characteristics

Parameter	Description	Note	Min.	Тур.	Max.	Unit
ADC	Resolution	Bypass mode		12		BITS
ADC_{BIT}	Resolution	Divided mode (1/3.3)		12		BITS
F _{CLK_ADC}	Clock Source	From digital			400	kHz
		Single-ended mode		11 E		LSB
ADC	DNL	(Bypass mode)		±1.5		LSB
ADC _{DNL}	DINE	Differential mode				1.00
		(Bypass mode)	:	±3.0		LSB
100		Single-ended mode		±1.0		LSB
	INII	(Bypass mode)		11.0		LSB
ADCINL	OC _{INL} INL	Differential mode		±2.0		LSB
		(Bypass mode)				LSB
		External channel	0		VBAT	V
ADCvin_range		(Divided Mode)	U		VBAI	
	Innut Valtaga Danga	External channel	0		1	
	Input Voltage Range	(Bypass Mode)	U		1	1
		Internal channel	1.8	0	3.63	V
		(VBAT)	1.0			V



ADC _{R_IN} Input Impedance	lance the lance of the same	Bypass mode	10M	Ohm
	Resistor divider mode (1/4)	500k	Ohm	
ADC _{C_Sample} Input Impedance -	Bypass mode	1.9	pF	
	iliput illipedance	Resistor divider mode (1/4)	1.9	pF

Radio Characteristics

General Radio Characteristics

Parameter	Description	Note	Min.	Тур.	Max.	Unit
F _{RANGE}	Frequency range		2402		2480	MHz

RX Performance

Condition: VBAT=3V, ambient temperature=25°C

Parameter	Description	Note	Min.	Тур.	Max.	Unit
P _{RX_MIN}	Sensitivity (LE 1M)	PER ≤ 30.8%	-97			dBm
P _{RX_MAX}	Maximum received power	PER ≤ 30.8%		-1		dBm
	C/I co-channel		21			dB
	C/I + 1MHz offset		15			dB
	C/I - 1MHz offset		15			dB
	C/I + 2MHz offset		-17			dB
CI_{RX_1M}	C/I - 2MHz offset		-15			dB
	C/I + 3MHz offset		-27			dB
	C/I image		-9			dB
	C/I image + 1MHz offset		-15			dB
	C/I image - 1MHz offset		-15			dB
	Dischar Davis	30MHz ~ 2000MHz	-30			dBm
D	Blocker Power	2003MHz ~ 2399MHz	-30			dBm
P_{RX_OOB}	Wanted signal level= -	2484MHz ~ 2997MHz	-30			dBm
	67dBm	3000MHz ~ 12.75GHz	-30			dBm
PER _{MAX}	Max PER report integrity	Wanted signal= -30dBm		50%		-
P _{RX_IMD}		Wanted signal f(0) = -64dBm				
	Max Intermodulation level	Worst intermodulation level	-50			dBm
	iviax intermodulation level	@2f1-f2=f0, f1-f2 =n MHz,				
		n=3,4,5				



TX Performance

Condition: VBAT=3V, ambient temperature=25°C

Parameter	Description	Note	Min.	Тур.	Max.	Unit
P _{TX_MAX}	Maximum output power				8	dBm
	Adia and alcount account	+2MHz			-20	dBm
D	Adjacent channel power	-2MHz			-20	dBm
P_{TX_ADJ}	ratio	≥ +3MHz			-30	dBm
	(LE 1M)	≤ -3MHz			-30	dBm
		Δf1avg		250		kHz
F _{MOD}	Modulation Characteristics	Δf2max	185			kHz
	(LE 1M)	Δf2max pass rate		100%		-
		Δf2avg / Δf1avg		0.88	/7	
	Camian for any affirm to a large	Average Fn		12.5		kHz
F	Carrier frequency offset and drift	Drift rate	K	10		kHz/50μs
F _{CAR_OFFSET}	2	Average drift		10		kHz/50μs
	(LE 1M)	Maximum drift		10		kHz/50μs
P _{TX_HD2}	2 nd harmonic power	101		-50		dBm
P _{TX_HD3}	3 rd harmonic power			-50		dBm

Digital I/O Pin DC Characteristics

Condition: ambient temperature=25°C

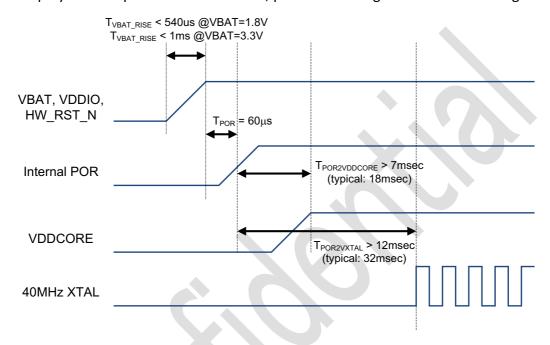
Parameter	Description	Note	Min.	Тур.	Max.	Unit
V _{IH33}	Input high voltage		2	3.3	3.6	V
V _{IL33}	Input low voltage	VDDIO=3.3V		0	0.9	V
V _{ОН33}	Output high voltage		2.97		3.3	V
V _{OL33}	Output low voltage		0		0.33	V
V _{IH28}	Input high voltage	VDDIO=2.8V	1.8	2.8	3.1	V
V _{IL28}	Input low voltage			0	0.8	V
V _{OH28}	Output high voltage		2.5			V
V _{OL28}	Output low voltage		0		0.28	V
	6. 6.	VDDIO=3.3V		10		kOhm
	Strong Pull	VDDIO=1.8V		20		kOhm
D	Weak Pull	VDDIO=3.3V		100		kOhm
R_pull	vveak Pull	VDDIO=1.8V		200		kOhm
	Strong Pull	VDDIO=3.3V		5		kOhm
	(P2_2~P2_7)	VDDIO=1.8V		2.5		kOhm



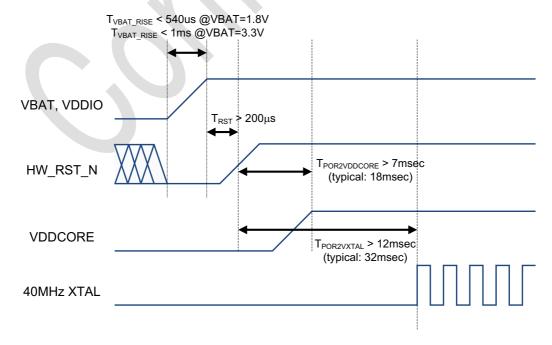
В	Weak Pull	VDDIO=3.3V	50			kOhm
R_{pull}	(P2_2~P2_7)	VDDIO=1.8V		25		kOhm
I _{IH}	Input high current	PAD configured as input			0.1	μΑ
I _{IL}	Input low current	mode			0.1	μΑ

Boot Sequence

Boot up by internal power on reset circuit, power on timing is shown in below figure.

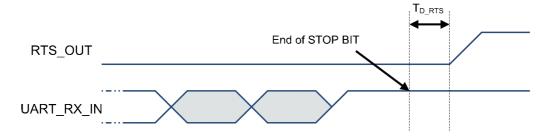


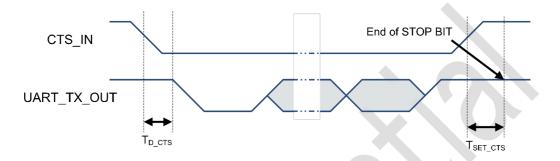
Boot up by HW RST N pin, power on timing is shown in below figure.





UART Characteristics

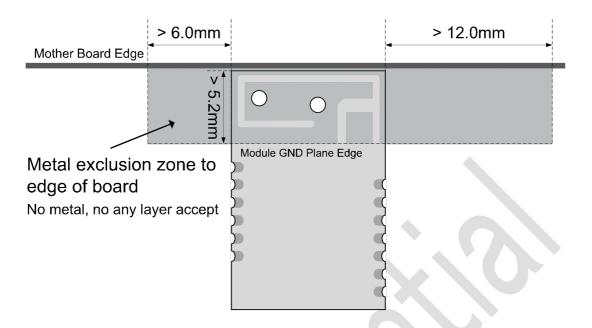




Parameter	Description	Note	Min.	Тур.	Max.	Unit
T_{D_RTS}	Timing between UART_RX_IN stop bit and RTS rising edge when RX FIFO is full				0.5	ns
T _{D_CTS}	Timing between CTS falling edge and UART_TX_OUT first bit				25	ns
T _{SET_CTS}	Timing between CTS rising edge and UART_TX_OUT stop bit		75			ns

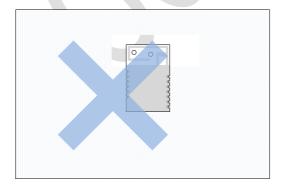


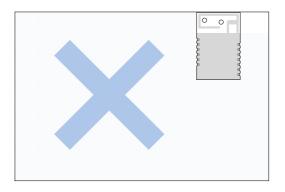
■ PCB LAYOUT GUIDE



Module Placement Example:

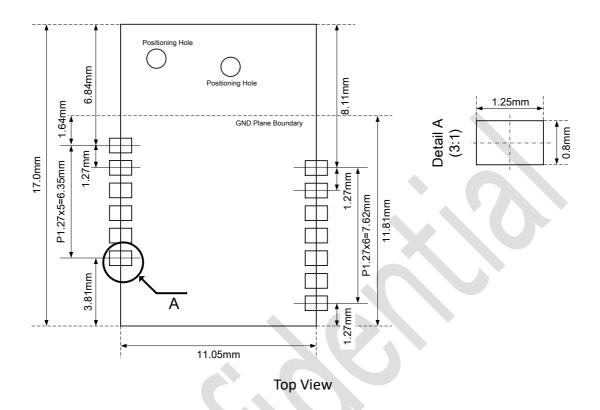








MODULE DIMENTIONS





BQB Certificate

FCC certificate











Japan Telecom

Antenna Test Report

