

## Bluetooth v5.1 dual-mode Module

### Description

The BM-8753BFR is a highly integrated single-chip Bluetooth 2.1/3.0/4.0/5.1 module with a UART interface. It combines a BT Protocol Stack (LM, LL, L2CAP, GATT, RFCOMM, SPP, and LE), BT Baseband, modem, and BT RF in a module.

The BM-8753BFR Bluetooth module complies with Bluetooth core specification v4.0/v5.1, and support dual mode (BR/EDR+Low Energy Controllers). It is compatible with previous versions, including v2.1+EDR. For BR/EDR, it allows one active link in either slave mode or master mode. For Low Energy, it supports multiple states and allows one active link a slave mode. A BR/EDR link and a LE link can be active at the same time.

The system-on-chip architecture design of the module makes a much smaller space and minimal cost and simplifies the whole system design.

### Features

- 16x10x1.95mm  
18-pin
- Complies with HS-UART with configurable baud rate for Bluetooth
- Compatible with Bluetooth v2.1 and v3.0 systems
- Supports Bluetooth 5.1 Low Energy (BLE)
- HS-UART interface for Bluetooth data

transmission compliant with H4 specification

- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports legacy pairing and secure simple pairing in BR/EDR and BLE
- Supports Low Power Mode (Sniff mode)
- Bluetooth 5.1 Dual Mode support: Simultaneous BLE and BR/EDR
- Supports multiple Low Energy states
- Supports SPP Profile
- Supports GATT Profile
- RoHS compliant

### Application

- Data Transparency

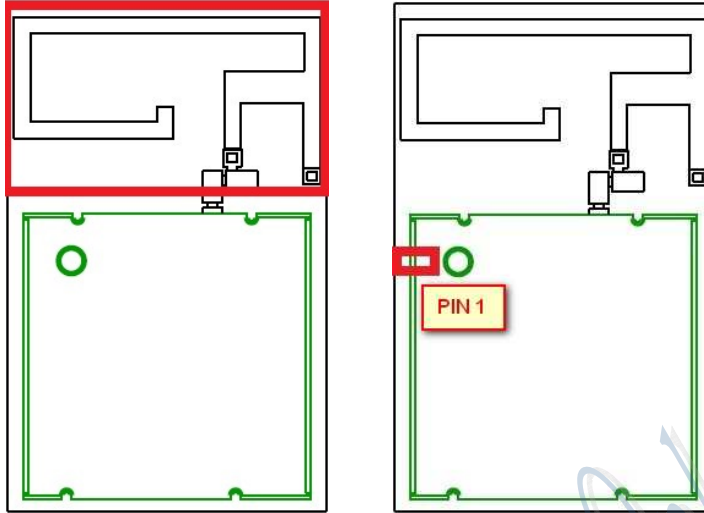
## Revision History

Version	Date	Change Description
1.0	12/02/2022	Initial release
1.1	12/09/2022	Addition Pin Definition
1.2	05/12/2023	Change dimension tolerance to $\pm 0.15\text{mm}$
1.3	06/12/2023	1. Change transmitter power to 7.5dBm 2. Addition recommend layout footprint

**Note :** All electrical and mechanical specifications may be changed by CC&C Technologies, Inc. without notice.

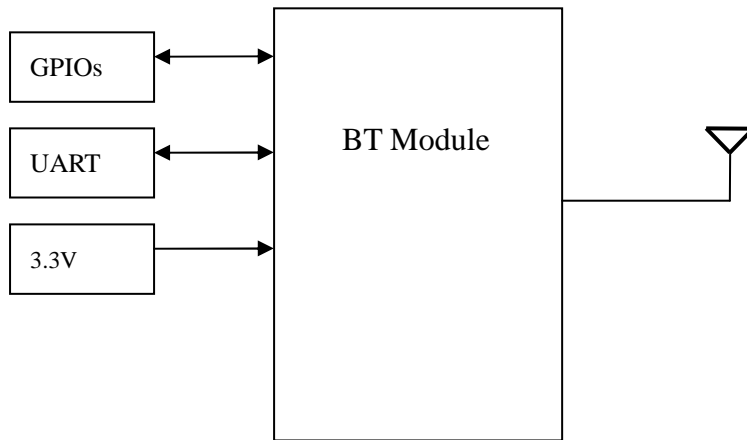
### Factory options

- RF output by PCB Antenna(RF type-1), DFN Pads(RF type-2)



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Functional Block Diagram



Block Diagram

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Pin Assignment (Top view)



## Pin Definition

Pin	Pin Name	Pad Type	Description
1	RF	A	RF output external Antenna (Type 2)
2	GND	Ground	
3	P1_0	IO PU	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> <li>● LDO_HV33 power domain</li> </ul>
4	P1_1	IO PU	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> <li>● LDO_HV33 power domain</li> </ul>
5	P3_0/RX	IO PU	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> <li>● LDO_HV33 power domain</li> <li>● UART_RX for flash memory programming</li> </ul>
6	P3_1/TX	IO PU	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> <li>● LDO_HV33 power domain</li> <li>● UART_TX for flash memory programming</li> </ul>
7	MFB	I_PU	Multi-function button input with internal pull high, low active with at least 3ms low
8	VD33	PI	Supply input 3.3V power
9	GND	Ground	
10	GND	Ground	
11	HW_RST_N	I_PU	System reset input with internal pull high, low active with a least 8ms low to trigger system reset
12	LDO_AUX	PO	Programmable linear regulator output for I/O
13	MODE	IO PU	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> <li>● LDO_AUX power domain</li> </ul> HCI mode selection H: APP mode L: HCI mode
14	P2_1	IO	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> <li>● LDO_AUX power domain</li> </ul>
15	P2_2	IO	Programmable GPIO <ul style="list-style-type: none"> <li>● Configurable pull high/low state</li> </ul>

			<ul style="list-style-type: none"> <li>● LDO_AUX power domain</li> </ul>
16	P0_0/ADC_0	IO IO A	Programmable GPIO <ul style="list-style-type: none"> <li>● Programmable as ADC input pin</li> <li>● Configurable pull high/low state</li> <li>● LDO_AUX power domain</li> </ul>
17	P0_1/ADC_1	IO IO A	Programmable GPIO <ul style="list-style-type: none"> <li>● Programmable as ADC input pin</li> <li>● Configurable pull high/low state</li> <li>● LDO_AUX power domain</li> </ul>
18	GND	Ground	

Pad Type	Definition
A	Analog
IO	Bidirectional digital pad
IO PU	Bidirectional digital pad with pull high resistor inside when input mode
IO A	Bidirectional digital pad and programmable ADC
PO	Power output
PI	Power input
I_PU	Input with internal pull high inside

**SPECIFICATION**

Product Name	Bluetooth 5.1 dual-mode Module
Model Number	E78
Operating Frequency	2402~2480 MHz
Transmitter power	7.5dBm
Receiver sensitivity	≤ -70dBm

**Power Voltage Range**

Symbol	Description	Min.	Typ.	Max.	Units
VD33	3.3V Supply Voltage	2.8	3.3	4.35	V
	Operating Temperature	0	25	60	°C

**Digital logic characteristics**

Item	Min.	Typ.	Max.	Unit
Input low voltage (Vil)	-0.4	-	0.4	V
Input high voltage (Vih)	0.7xVDDIO	-	VDDIO+0.4	V
Output low voltage (VDDIO=1.8V)	-	-	0.2	V
Output high voltage (VDDIO=1.8V)	VDDIO-0.2	-	-	V
Output low voltage (VDDIO=3V)	-	-	0.4	V
Output high voltage (VDDIO=3V)	VDDIO-0.4	-	-	V

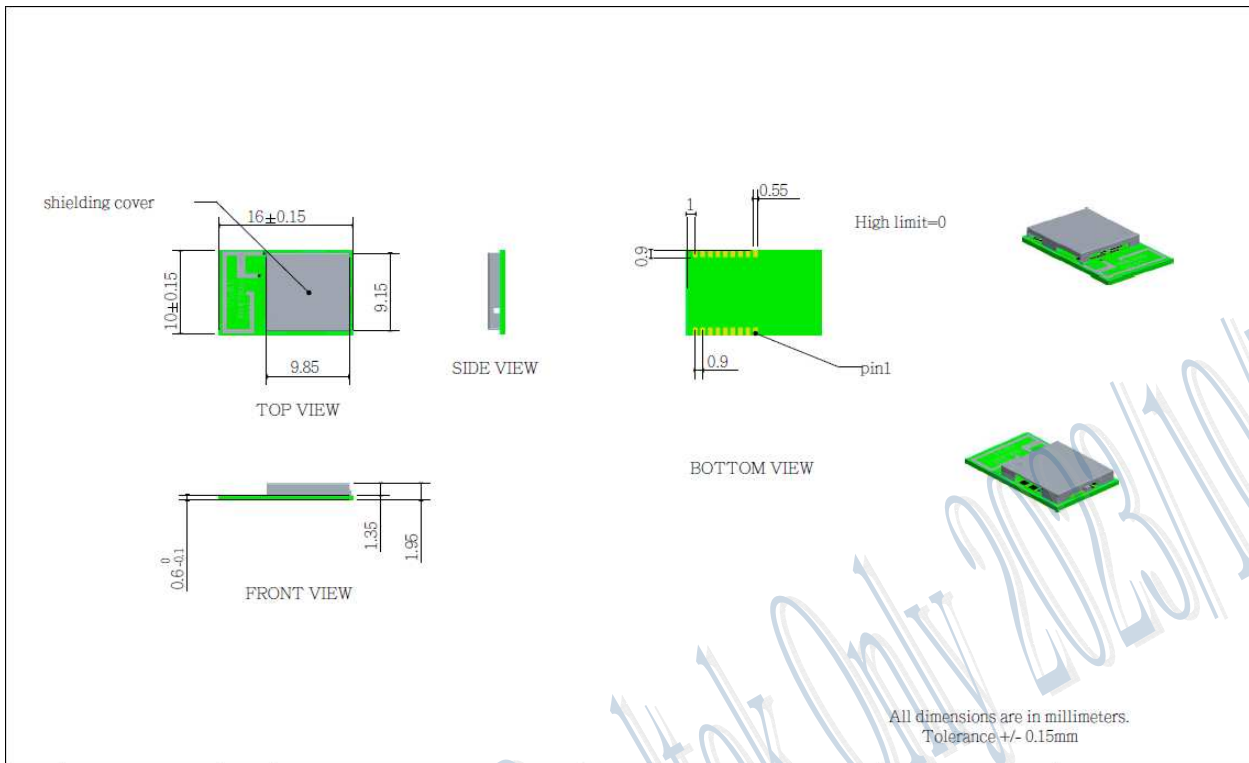
VDDIO is LDO\_AUX or LDO\_HV33, GPIO power domain, check the pin description.

**Internal Low Drop Linear Regulator – LDO\_AUX**

Item	Min.	Typ.	Max.	Unit
Output voltage	1.8	-	3.6	V
Output current	-	-	100	mA

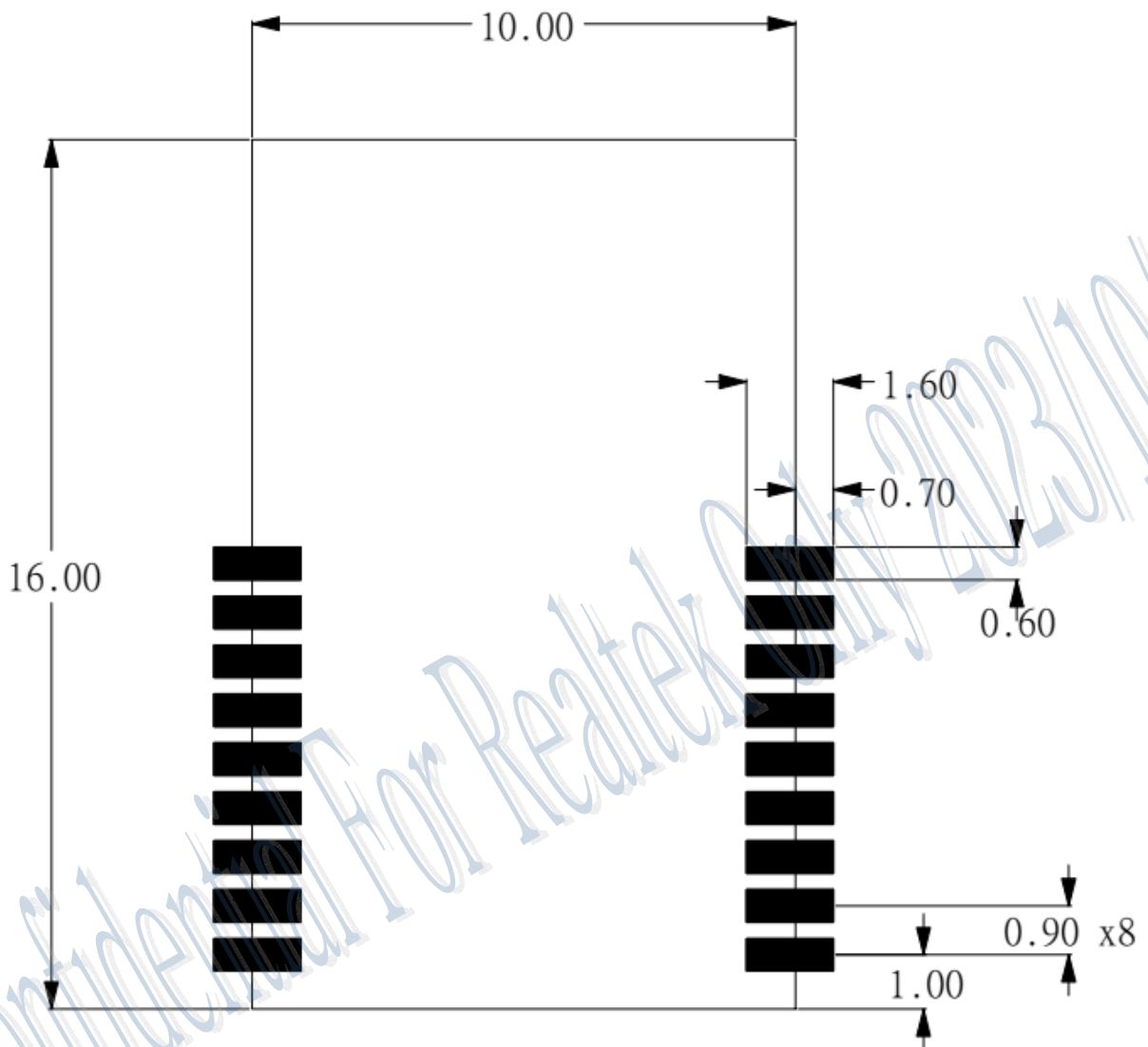


**Module dimension**



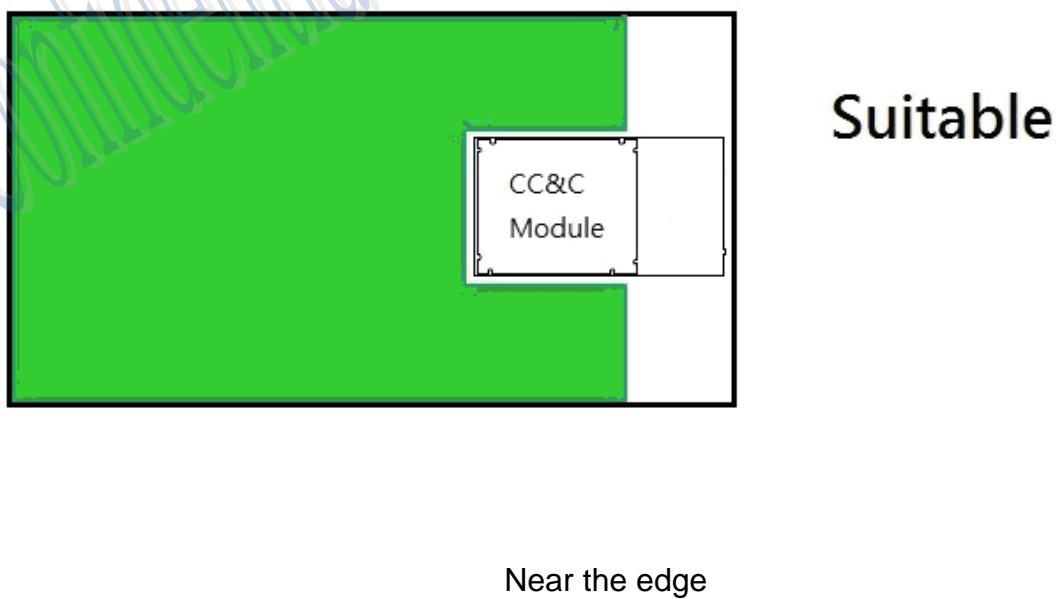
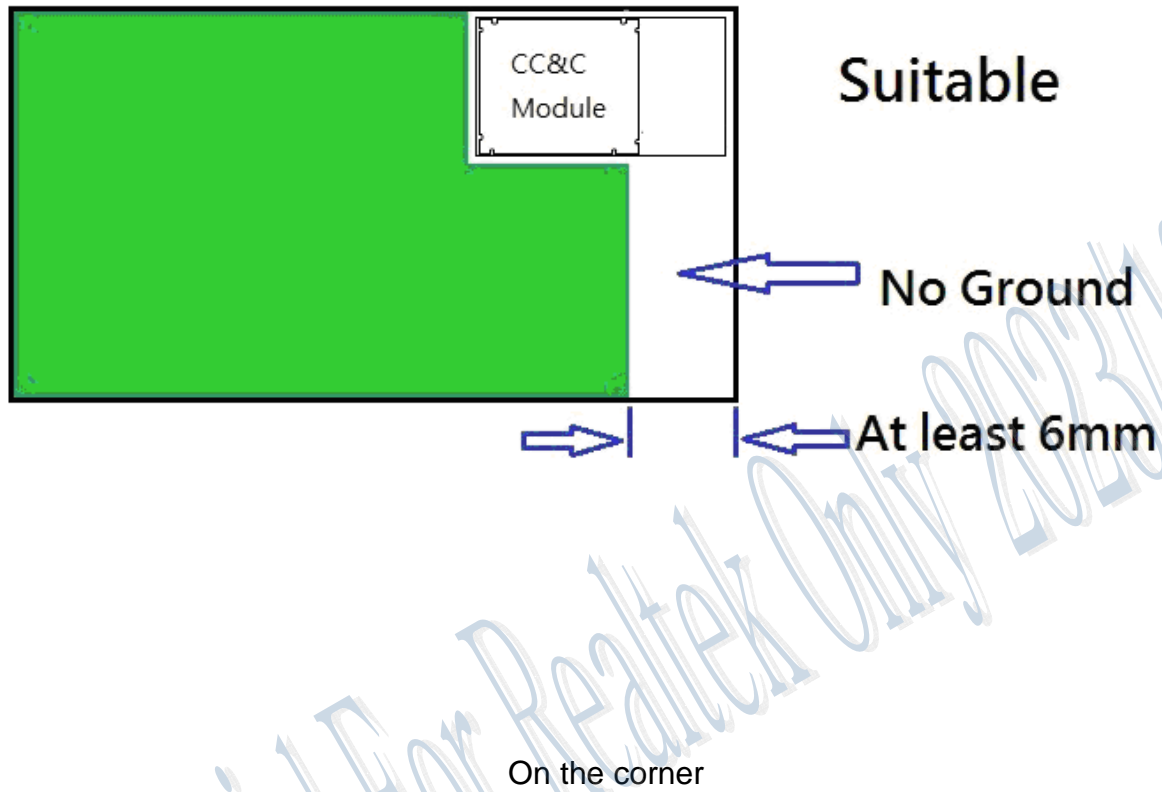
			CC & C TECHNOLOGIES, INC.							SCALE		DESCRIPTION: E78		MODEL NO.		APPROVAL	
										QTY				DWG NO.		DESIGNED jeff	
										MATERIAL		FINISH		PARTS NO.		DRAWING jeff	
ITEM	DESCRIPTION	DATE	TOL	0-6	6-30	30-80	80-180	180-315	315-800	UNIT	DWG	PCS	SET				
			0.05	0.1	0.15	0.2	0.25	0.3	MM	REV.							

Recommend layout footprint

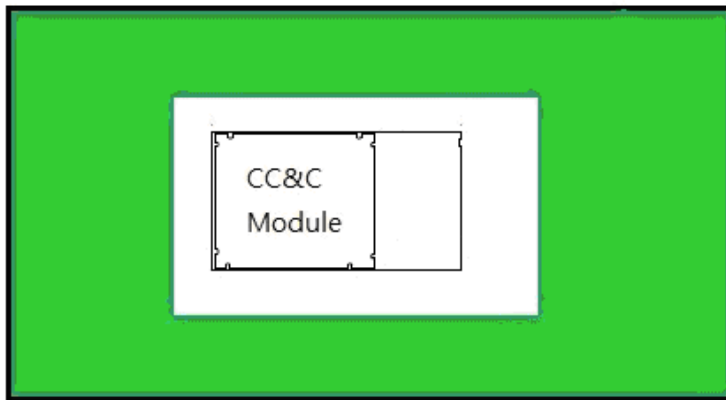


### Placement Guideline

It is recommended that module be placed on the corner of the main board or near the edge as shown below.



However, placing module inside the main board affects the RF performance and may reduce the RF range significantly.

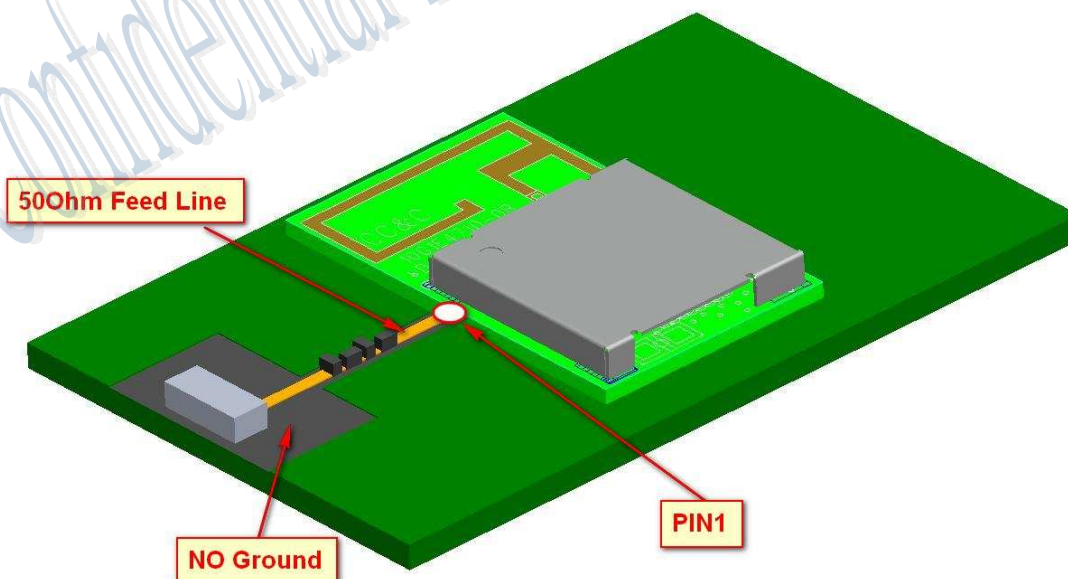


Unsuitable

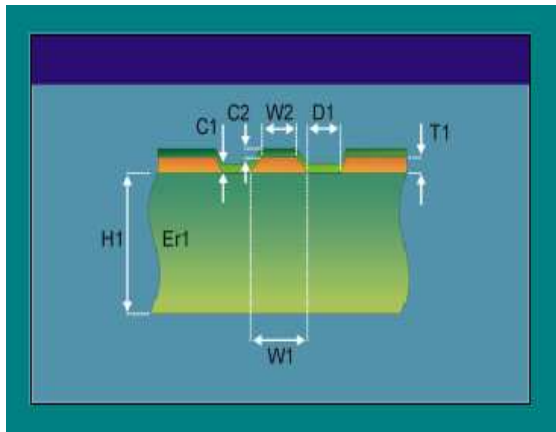
## RF out

RF type-2

Please have the impedance of feed lines to be 50 ohms from RF output pin to antenna.



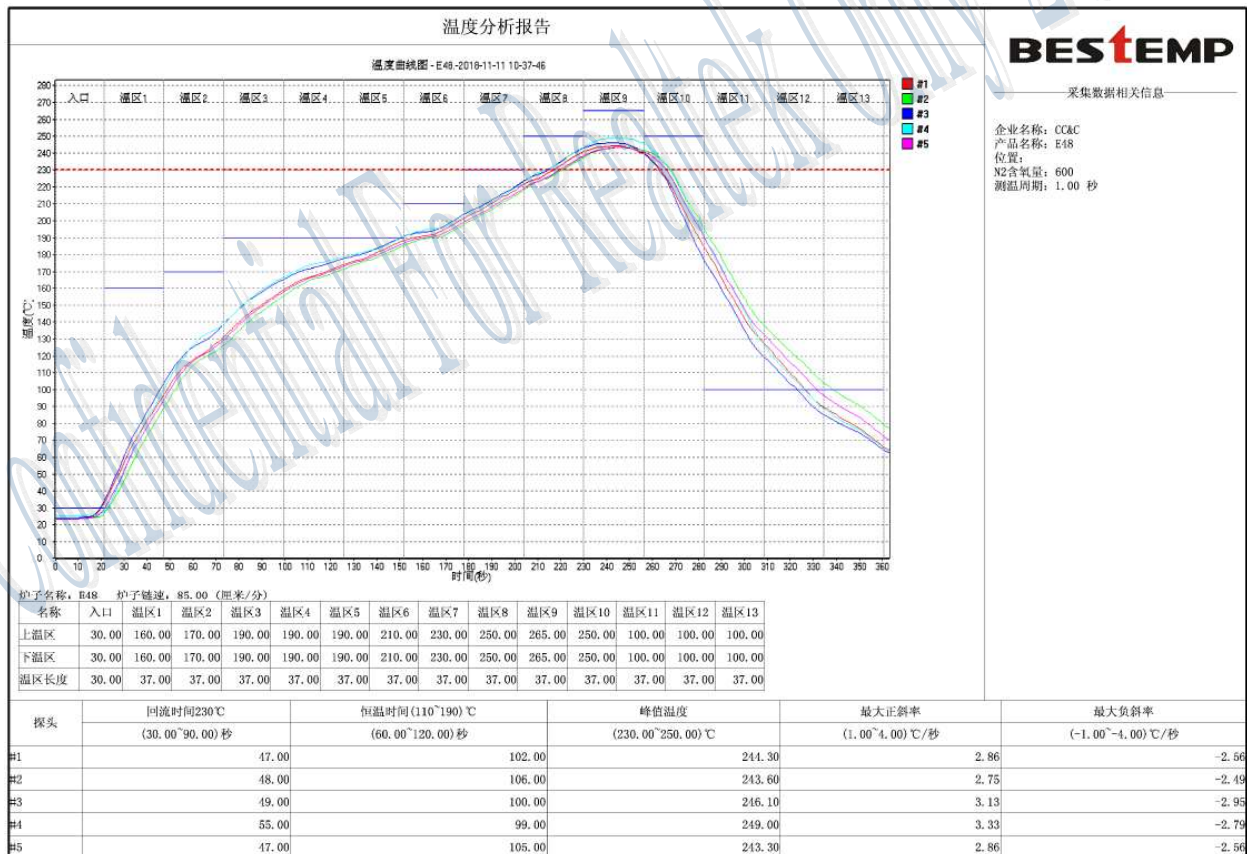
50 Ohm Feed Line:



- H1: 30 ~ 60 mil
- Er1: 4.2
- W1: 20 mil
- W2: 20 mil
- D1: 5 mil
- C1: 0.7 mil
- C2: 0.7 mil
- T1: 1.4 mil (1 oz)

Impedance: 51 ~ 53 Ohm

### Reference – Temperature Reflow Chart



Reflow Notice:

1. If the system PCBA is double side design, please reflow the side without this module first.
2. Don't let the solder machine temperature over 250°C or follow solder paste vendors's recommended temperature.
3. The Ramp-up temperature speed is 1-4°C per second, the Ramp-down temperature speed is 1-4°C per second.
4. This temperature reflow chart is for reference only, it depends on the manufacturing machine's

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 characters requirement.

This module is surface mount device; please refer below conditions for drying before solder reflow processes. (extracted from IPC/JEDEC J-STD-033B.1)

Bake @ 125 °C		Bake @ 90 °C		Bake @ 40 °C	
Exceeding floor Life By > 72h	Exceeding floor Life By ≤ 72h	Exceeding floor Life By > 72h	Exceeding floor Life By ≤ 72h	Exceeding floor Life By > 72h	Exceeding floor Life By ≤ 72h
9 hours	7 hours	33 hours	23 hours	13 days	9 days

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